THIN FILM TRANSISTOR ARRAY PANEL USED FOR A LIQUID CRYSTAL DISPLAY AND A MANUFACTURING METHOD THEREOF

BACKGROUND OF THE INVENTION

A. Field of the Invention

The present invention relates to a thin film transistor (TFT) array panel used for a liquid crystal display (LCD) and a fabricating method thereof. More particularly, the present invention relates to a method for manufacturing a TFT array panel through a photolithography process of four steps and a TFT array panel manufactured thereby.

B. Description of the Conventional Art

Generally, a liquid crystal display (LCD) includes two panels and liquid crystal material injected therebetween. Referring to FIG. 1, a wiring such as gate lines (not shown) and data lines (not shown), a pixel electrode 70 and a thin film transistor 70 are formed in either panel 100 of two panels. In addition, a black matrix 210, a color filter 220 and a common electrode 240 are formed in the other panel, and an overcoat film 230 is formed between the black matrix 210 and the color filter 220, and the common electrode 240.

Hereinafter, a conventional thin film transistor (TFT) array panel will be explained in detail with reference to FIGS. 2 and 3.

FIG. 2 is a plan view illustrating a conventional TFT array panel used for a liquid crystal display (LCD) and FIG. 3 is a cross-sectional view cut along the line III-III in FIG. 2.

As shown in FIG. 1 and FIG. 2, a gate line 11 and its branch, a gate electrode 12, are formed on a substrate 100. The gate line 11 and the gate electrode 12 are covered with a gate insulating layer 20. An amorphous silicon layer 30 and an n^+ amorphous silicon layer 40 are formed on the gate insulating layer 20. A pixel electrode 70 separated from the amorphous silicon layer 30 and the n^+ amorphous silicon layer 40 is formed on the gate insulating layer 20. A data line 51 and a source electrode 52, as well as a drain electrode 53, are formed thereon and the drain electrode 53 is connected to the pixel electrode 70. They are all covered with a passivation layer 61, except the pixel electrode 70. A light shielding film 62 is formed over the TFT which includes the amorphous silicon layer 30, the n^+ amorphous silicon layer 40, the gate electrode 12, and the source and the drain electrodes 12 and 13. The light shielding film 62 is made in order to prevent the leakage current in the amorphous silicon layer 30.

FIGs. 4A to 4G are plan views illustrating a manufacturing process of the conventional TFT array panel shown in FIGs. 2 and 3.

Referring to FIG. 4A, metal such as Cr, Al and Ta

is deposited to a thickness of about 200 to 400 nm and patterned to form a gate line 11 and a gate electrode 12 through a photolithograph process using a first mask.

Referring to FIG. 4B, an insulating layer 20 of SiNx or SiO_2 is deposited to a thickness of about 300 to 400 nm, and an amorphous silicon layer 30 and an n^+ amorphous silicon layer 40 are deposited in sequence. The thickness of the amorphous silicon layer 30 is 200 nm and the thickness of the n^+ amorphous silicon layer 40 is 50 nm. Then, the amorphous silicon layer 30 and the n^+ amorphous silicon layer 40 are patterned in the same shape using a second mask.

Next, referring to FIG. 4C, an indium tin oxide (ITO) layer is deposited to a thickness of about 50 nm, and patterned to form a pixel electrode 70 through the photolithograph process using a third mask.

Referring to FIG. 4D, a conductive layer such as Cr, Ta or Ti is deposited to a thickness of about 150 to 300 nm, and patterned to form a data line 51 and a source and a drain electrodes 52 and 53 thorough the photolithography using a fourth mask.

Referring to FIG. 4E, the n^+ amorphous silicon layer 40 is etched to expose the amorphous silicon layer 30 on the gate electrode 12 using the data line 51 and a source and a drain electrodes 52 and 53 as a mask.

Referring to FIG. 4F, a passivation layer 61 of

SiNx is deposited and patterned. The thickness of the passivation layer 61 is in the range from 200 to 400 μm, and the portion of the passivation layer 61 on the pixel electrode 70 is removed, using a fifth mask.

Referring to FIG. 4G, photoresist is deposited to the thickness of about 0.5 to 3 μm and patterned to form a light shielding film 62 on the TFT through the photolithography process, using a sixth mask.

As described above, six masks are required with the exception of a pad, when fabricating the conventional TFT array panel. Furthermore, more than six masks are needed when considering the pad portion. Accordingly, the conventional method has disadvantages in that the fabrication method is complex and the manufacturing cost is high.

SUMMARY OF THE INVENTION

Accordingly, an object of the present invention is to reduce the number of photolithography steps, thereby reducing manufacturing cost and improving the productivity.

After patterning a passivation film and a light shielding film or a passivation film also having a function of the light shielding film in the present invention, the number of mask is reduced by etching a semiconductor layer, using the patterned film as a mask.

This will be explained in detail hereinafter.

A gate line and a gate electrode are formed on a substrate, and a gate insulating layer and a semiconductor layer are deposited in sequence. A data line, a source electrode and a drain electrode are formed through a photolithography step, after depositing a metal layer. The passivation film and the light shielding film or a passivation film of opaque material are deposited in sequence and patterned through the photolithography step. Here, the passivation film covers over the data line, the source electrode and a part of the drain electrode. A pixel electrode is formed by depositing transparent conductive material and etching the transparent conductive material through the photolithography step, after etching the semiconductor layer, using the passivation film as the mask.

In the present invention, only four masks are required when fabricating a thin film transistor (TFT) array panel with the exception of a pad. The pattern of the semiconductor layer is the same as the passivation film except a portion under the drain electrode, which is not covered with the passivation film.

To fabricate a panel with four masks including the pad, a step for etching only the gate insulating layer for exposing the pad, should be omitted. For this, it is preferable that the pattern of the gate insulating layer should be the same as the semiconductor layer and

the gate insulating layer is patterned, using the semiconductor layer as the mask. For this, the portions that the gate insulating layer should cover, that is, the gate line and the gate electrode are covered with the passivation film and the semiconductor layer, and the passivation film on the pad is etched to expose the pad when etching the passivation film.

Additional objects and advantages of the invention are set forth in part in the description which follows, and in part will be obvious from the description, or may be learned by practice of the invention. The objects and advantages of the invention will be realized and attained by means of the elements and combinations particularly pointed out in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, illustrate three embodiments of the invention and, together with the description, serve to explain the principles of the invention.

In the drawings:

FIG. 1 is a cross-sectional view illustrating a conventional liquid crystal display;

FIG. 2 is a plan view illustrating a conventional TFT array panel used for an LCD;

FIG. 3 is a cross-sectional view cut along the line III-III in FIG. 2;

FIGs. 4A to 4G are plan views illustrating a manufacturing process of the conventional TFT array panel shown in FIGs. 2 and 3;

FIG. 5 is a plan view illustrating a TFT array panel used for an LCD in accordance with a first preferred embodiment of the present invention;

FIG. 6 is a cross-sectional view cut along the line VI-VI in FIG. 5;

FIGs. 7A to 7G are plan views illustrating a fabrication process of a TFT array panel shown in FIGs. 5 and 6;

FIGs. 8A to 8G are cross-sectional views cut along the line VIII-VIII in FIGs. 7A to 7G;

FIG. 9 is a plan view illustrating a TFT array panel used for an LCD in accordance with a second preferred embodiment of the present invention;

FIG. 10 is a cross-sectional view cut along the line X-X in FIG. 9;

FIG. 11 is a cross-sectional view cut along the line XI-XI in FIG. 9;

FIG. 12 is a cross-sectional view cut along the line XII-XII in FIG. 9;

FIGs. 13A to 13C are plan views illustrating a fabrication process of a TFT array panel shown in FIGs. 9 to 12;

FIG. 14 is a plan view illustrating a TFT array panel used for an LCD in accordance with a third preferred embodiment of the present invention;

FIG. 15 is a cross-sectional view cut along the line XV-XV in FIG. 14;

FIG. 16 is a cross-sectional view cut along the line XVI-XVI in FIG. 14;

FIGs. 17A to 17C are plan views illustrating a fabrication process of a TFT array panel shown in FIGs. 14 to 16; and

FIG. 18 is a cross-sectional view illustrating a liquid crystal display in accordance with a preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made in detail to preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

FIG. 5 is a plan view illustrating a TFT array panel used for an LCD in accordance with a first preferred embodiment of the present invention and FIG. 6 is a cross-sectional view cut along the line VI-VI of FIG. 5.

As shown in FIGs. 5 and 6, a gate line 11 is formed horizontally on a substrate 100, and a branch vertically extended from the gate line 11, that is, a gate electrode 12, is formed on the substrate 100. The gate line 11 and the gate electrode 12 are covered with a gate insulating layer 20. A semiconductor layer of such as an amorphous silicon layer 30 and a doped semiconductor layer of such as an n^+ amorphous silicon

layer 40 are formed on the gate insulating layer 20. A data line 51 and a source electrode 52, as well as a drain electrode 53, are formed thereon in the same shape as the n^+ amorphous silicon layer 40. Here, the data line 51 is formed vertically, the branch extended horizontally therefrom, the source electrode 52 overlaps a part of the gate electrode 12, and the drain electrode 53 is formed symmetrically with the source electrode 53 for the gate electrode 12. They are all covered with a passivation film 61 and a light shielding film 62 having the same pattern as the passivation film 61, and a part of the drain electrode 53 is exposed outward the passivation film 61 and the light shielding film 62. Here, the pattern of the amorphous silicon layer 30 is the same as the passivation film 61 and the light shielding film 62 except a portion under the drain electrode 53 exposed outward the passivation film 61 and the light shielding film 62, and the pattern of the amorphous silicon layer 30 in the portion under the exposed drain electrode 53 is the same as the drain electrode 53. On the other hand, the pixel electrode 70 is formed on the gate insulating layer 20 exposed outward the passivation film 61 pattern, and connected to the exposed drain electrode 53. In addition, the pixel electrode 70 overlaps the gate line 11 via the gate insulating layer 20, and this portion functions as a storage capacitor.

Here, the light shielding film 62 may be formed

under the passivation film 61, and the passivation film 61 can be formed on the passivation film 61. In addition, a passivation film also having the function of the light shielding film may be formed, using opaque material of such as a black photoresist instead of forming the passivation film 61 and the light shielding film 62.

Since the amorphous silicon layer 30 is covered with the drain electrode 53 made of the light shielding film 62 or opaque metal, the leakage current in the amorphous silicon layer 30 is reduced. In addition, since the width of the pattern of the light shielding film is wider than that of the data line 51, the source and the drain electrodes 52 and 53, short-circuit between the data line and a common electrode (reference numeral 240 in FIG. 1) of a opposite panel (reference numeral 200 in FIG. 1) hardly occurs.

FIGs. 7A to 7G are plan views illustrating a fabrication process of a TFT array panel shown in FIGs. 5 and 6, and FIGs. 8A to 8G are cross-sectional views cut along the line VIII-VIII in FIGs. 7A to 7G.

Referring to FIGs. 7A and 8A, conductive material such as Cr, Al and Ta is deposited to a thickness of about 200 to 400 nm on a substrate 100 and patterned to form a gate line 11, a gate electrode 12 through a photolithography step, using a first mask. Here, the conductive material may be formed by a lower layer of Al or an alloy of Al-Nd and an upper layer of Mo,

instead of the single layer. In addition, the conductive material may be formed by a lower layer of Cr and an upper layer of the alloy of Al-Nd.

Referring to FIGs. 7B and 8B, an gate insulating layer 20 of such as SiNx and SiO_2 is deposited to a thickness of about 300 to 400 nm, and an amorphous silicon layer 30 and an n^+ amorphous silicon layer 40 are deposited in sequence thereon. The thickness of the amorphous silicon layer 30 is 200 nm and the thickness of the n^+ amorphous silicon layer 40 is 50 nm.

Next, referring to FIGs. 7C and 8C, a conductive layer of such as Cr, Ta or Ti is deposited to a thickness of about 150 to 300 nm, and patterned to form a data line 51, a source electrode 52 and a drain electrode 53 through the photolithography step, using a second mask.

Referring to FIGs. 7D and 8D, the exposed n^+ amorphous silicon layer 40 is etched, using the data line 51, the source electrode 52 and the drain electrode 53 as the mask.

Referring to FIGs. 7E and 8E, the passivation film 61 of such as SiNx is deposited to the thickness of 200 to 400 μm.

Referring to FIGs. 7F and 8F, and photoresist is deposited to a thickness of about 0.5 to 3 μm, and patterned to form the light shielding film 62. And the passivation film 61 is etched, using the light

shielding film 62 as the mask. In this process, the data line 51 and the source electrode 52 are covered with the light shielding film 62 and the passivation film 61, and a part of the drain electrode 53 is exposed. Then, the amorphous silicon layer 30 is etched, using the light shielding film 62 and the passivation film 61 and the exposed drain electrode 53 as the mask.

Here, the light shielding film 62 may be formed by a conductive material such as Cr.

Finally, referring to FIGs. 7G and 8G, an indium tin oxide (ITO) layer is deposited to a thickness of about 50 nm, and patterned to form a pixel electrode 70 through the photolithography step, using a fourth mask.

As described above, the effect of the TFT array panel for an LCD in accordance with the first preferred embodiment of the present invention lies in that two masks are reduced, thereby reducing manufacturing cost and also increasing productivity by fabricating the TFT array panel using only four masks, compared to the conventional method.

A method for fabricating a panel including a pad using only four masks, and a structure fabricated thereby, are suggested in a second preferred embodiment of the present invention.

FIG. 9 is a plan view illustrating a TFT array panel used for an LCD in accordance with the second preferred embodiment of the present invention, and FIG.

9 illustrates also a gate pad and a data pad.

The main difference between the first preferred embodiment and the second preferred embodiment lies in that the gate insulating layer 20 has the same pattern as the amorphous silicon layer 30. Of course, likewise the first preferred embodiment of the present invention, the pattern of the amorphous silicon layer 30 is the same as the passivation film 60 also having the function of the light shielding film except for a portion under the drain electrode 53 exposed outward the passivation film 60 having the light shielding film, and the pattern of the amorphous silicon layer 30 in the portion under the exposed drain electrode 53 is the same as the drain electrode 53.

On the other hand, since the gate insulating layer 20 should cover the gate line 11, the gate electrode 12 and the gate pad 13, the pattern of the passivation film 60, the amorphous silicon layer 30 and the gate insulating layer 20 is formed on the gate line 11, the gate electrode 12 and the gate pad 13, except on the data line 51 and the source electrode 52, and a part of the drain electrode 53.

In addition, the passivation film 60, the amorphous silicon layer 30 and the gate insulating layer 20 have contact holes 14 and 15 on the gate pad 13 and a data pad 54 since the gate pad 13 and the data pad 54 are electronically connected to the outside and exposed to the outside. Here, a gate ITO pad 71 and a

data ITO pad 72 connected respectively to the gate pad 13 and the data pad 54 through the contact holes 14 and 15 are formed to prevent oxidization which occurs when the gate pad 13 and the data pad 54 are directly exposed to the outside. Besides these, the differences between the first and the second preferred embodiments of the present invention lie in that the gate line 11, the gate electrode 12 and the gate pad 13 are formed in two layers respectively, and one layer of the passivation layer 60 of the black photoresist, also having the function of the light shielding film, is added. These layers may be formed in a single layer or in two layers.

The structure in FIG. 9 will be explained in detail.

FIG. 10 is a cross-sectional view cut along the line X-X in FIG. 9.

Referring to FIG. 10, the gate line 11 and the gate electrode 12 are made of respectively lower layers 111 and 121 and upper layers 112 and 122. The pattern of the gate insulating layer 20 is the same as the amorphous silicon layer 30. On the other hand, the gate insulating layer 20, the amorphous silicon layer 30 and the passivation film 60 cover the gate line 11 of two layers, and a pixel electrode 100 overlaps thereon.

The sections of the gate pad 13 and the data pad 54 will be explained.

FIG. 11 is a cross-sectional view cut along the line XI-XI in FIG. 9.

Referring to FIG. 11, the gate pad 13 is formed by a lower layer 131 and an upper layer 132, and the gate pad 13 is exposed by the contact hole 14 formed on the gate insulating layer 20, the amorphous silicon layer 30 and the passivation film 60. In addition, the upper layer 132 of the gate pad 13 is covered with the gate ITO pad 71.

FIG. 12 is a cross-sectional view cut along the line XII-XII in FIG. 9.

Referring to FIG. 12, the gate insulating layer 20, the amorphous silicon layer 30 on the gate insulating layer 20, an n^+ amorphous silicon layer 40 on the amorphous silicon layer 30, and the data pad 54 on the n^+ amorphous silicon layer 40 are formed in the same pattern, and are connected to the ITO pad 72 through the contact hole formed in the passivation film 60 which covers the above pattern.

The above-mentioned TFT array panel in accordance with the second preferred embodiment of the present invention is formed primarily in the same way as the first preferred embodiment of the present invention. FIGs. 13A to 13C are plan views illustrating a fabrication process of a TFT array panel shown in FIGs. 9 to 12. The left portions in FIGs. 13A to 13C correspond to the TFT and the gate line in FIG. 10, central portions correspond to the gate pad in FIG. 11,

and the right portions correspond to the data pad in FIG. 12.

First, referring to FIG. 13A, two layers of metal are deposited in sequence, and patterned to form the gate line 11, the gate electrode 12 and the gate pad 13, using a first mask. The lower layer and the upper layer may be formed by AL-Nd and Mo, or Cr and Al-Nd. In the second preferred embodiment of the present invention, the lower layer and the upper layer is formed by AL-Nd and Mo. Next, the gate insulating layer 20, the amorphous silicon layer 30, the n^+ amorphous silicon layer 40 and a metal layer 50 are deposited in sequence.

FIG. 13B, the metal layer 50 is patterned to form the data line 51, the source electrode 52, the drain electrode 53 and the data pad 54, using a second mask. The n^+ amorphous silicon layer 40 is etched, using the patterned data line 51, the source electrode 52, the drain electrode 53 and the data pad 54 as the mask. After that, the passivation film 60 is deposited.

Referring to FIG. 13C, the passivation film 60 is patterned, using a third mask. Here, the passivation film 60 covers the gate line 11, the gate electrode 12, the gate pad 13, the data line 51, the source electrode 52, the drain electrode 53 and the data pad 54. The contact holes 14 and 55 are formed on central portions of each pad 103 and 114, and an upper portion of a part of the drain electrode 53 is removed. The amorphous

silicon layer 30 and the gate insulating layer 20 are etched in sequence, using the patterned passivation film 60 as the mask. Here, the amorphous silicon layer 30 and the gate insulating layer 20 under the drain electrode 53 are not etched.

Finally, the ITO film is deposited and patterned to form the pixel electrode 70, the gate ITO pad 71 and the data ITO pad 72, using a fourth mask, as illustrated in FIGs. 10, 11 and 12.

In the second preferred embodiment of the present invention, the pixel electrode 70 can be defective since the height difference in a portion in which the pixel electrode 70 overlaps the gate line 11, is large, as illustrated in FIG. 10.

A third preferred embodiment of the present invention suggests a structure which can reduce the height difference in the portion in which the pixel electrode 70 overlaps the gate line 11.

FIG. 14 is a plan view illustrating a TFT array panel used for an LCD in accordance with a third preferred embodiment of the present invention, and FIG. 15 is a cross-sectional view cut along the line XV-XV in FIG. 14.

Referring to FIG. 14, the passivation film 60, which is made of opaque material and also serves as the light shielding function covers even the drain electrode 53 completely. Instead, the passivation film 60 has a contact hole 56 exposing the drain electrode

53, and the pixel electrode 70 contacts the drain electrode 53 through the contact hole 56.

In addition, the structure in FIG. 14 has the effects that storage capacitance is formed through the connection portion and the height difference of the pixel electrode 70 is reduced by forming a connection portion made of the same material as the data line 51, instead that the gate line 11 directly overlaps the pixel electrode 70. That is, referring to FIG. 15, the n^+ amorphous silicon layer 40 and a connection portion 57 are formed, overlapping the gate line 11 on the amorphous silicon layer 30 formed on the gate line 11. The connection portion 57 is exposed outside the passivation film 60 and connected to the pixel electrode 70. The passivation film 60 in this portion is formed in the same way as the first and the second preferred embodiments of the present invention, the insulating layer 20 and the amorphous silicon layer 30 under the passivation film 60 are formed a little different from the passivation film 60 since the insulating layer 20 and the amorphous silicon layer 30 are formed even under the connection portion 57 exposed outside the passivation film 60. On the other hand, the pixel electrode 70 has the height difference from the upper portion of the connection portion 57 to the substrate 100, and compared to the second preferred embodiment of the present invention, this is the reduced hight difference, considering that the

passivation film 60 is thicker than the n^+ amorphous silicon layer 40 and the connection portion 57.

On the other hand, the structure of the data pad 54 in accordance with the third preferred embodiment of the present invention is the same as the first preferred embodiment of the present invention, but the structure of the gate pad 13 is a little different from that in accordance with the first preferred embodiment of the present. The structure of the gate pad 13 in accordance with the third preferred embodiment of the present invention will be explained hereinafter.

FIG. 16 is a cross-sectional view cut along the line XVI-XVI in FIG. 14.

Referring to FIG. 16, the gate pad 13 are formed by a lower layer 131 and an upper layer 132, but the gate pad 13 is exposed through a contact hole 55 formed in the passivation film 60, the amorphous silicon layer 30 and the gate insulating layer 20, and an upper layer 132 of a portion contacting a gate ITO pad 71 is etched. This is why the lower layer 131 is made of Cr and the upper layer 132 is made of alloy of Al-Nd in the third preferred embodiment of the present invention. The gate ITO pad should cover the Al or the alloy of Al-Nd since Al or the alloy is easy to be oxidized and rust, but the upper layer 132 is etched since the ITO and the Al alloy do not contact each other well and an oxidation film is formed on a surface, whereby resistance becomes large.

Hereinafter, a fabrication process of a TFT array panel in accordance with the third preferred embodiment of the present invention will be explained with reference to FIGs. 17A to 17C. Here, the left portions in FIGs. 17A to 17C correspond to the TFT and the gate line in FIG. 15, central portions in FIGs. 17A to 17C correspond to the gate pad in FIG. 16, and the right portions in FIGs. 17A to 17C correspond to the data pad in FIG. 12.

First, referring to FIG. 17A, two layers of metal are deposited in sequence, and patterned to form the gate line 11, the gate electrode 12 and the gate pad 13, using a first mask. The lower layer and the upper layer is formed by Cr and Al-Nd. Next, the gate insulating layer 20, the amorphous silicon layer 30, the n^+ amorphous silicon layer 40 and a metal layer 50 are deposited in sequence.

FIG. 17B, the metal layer 50 is patterned to form the data line 51, the source electrode 52, the drain electrode 53, the data pad 54 and a connection portion 57, using a second mask. The n^+ amorphous silicon layer 40 is etched, using the patterned data line 51, the source electrode 52, the drain electrode 53, the data pad 54, and the connection portion as the mask. After that, the passivation film 60 is deposited.

Referring to FIG. 17C, the passivation film 60 is patterned, using a third mask.. Here, the passivation film 60 covers the gate line 11, the gate electrode 12,

the gate pad 13, the data line 51, the source electrode 52, the drain electrode 53 and the data pad 54. The contact holes 14, 55 and 56 are formed on central portions of each pad 103 and 114 and the drain electrode 53, and an upper portion of a part of the connection portion 57 is removed. The amorphous silicon layer 30 and the gate insulating layer 20 are etched in sequence, using the patterned passivation film 60 as the mask. Here, the amorphous silicon layer 30 and the gate insulating layer 20 under the connection portion 57 are not etched. Next, the upper portion of the exposed gate pad 13 is etched by the contact hole 14.

Finally, the ITO film is deposited and patterned to form the pixel electrode 70, the gate ITO pad 71 and the data ITO pad 72, using a fourth mask, as illustrated in FIGs. 15, 16 and 12.

On the other hand, there is no need to form the light shielding film additionally on an upper substrate since the passivation film 60 also having the function of the light shielding film covers the border of the pixel and the TFT in the second and the third preferred embodiments of the present invention. That is, as illustrated in FIG. 18, a wiring (not shown), the pixel electrode 70, the TFT and the passivation film also having the function of the light shielding film are formed in a lower substrate 100. The light shielding film is not needed in the other substrate, and only a

color filter 220, a common electrode 240, and an overcoat 230 are formed in the other substrate.

As described above, the effect of the present invention lies in that manufacturing cost can be reduced and the productivity is improved since the process is reduced to four steps by patterning the light shielding film and the passivation film, which have the same pattern each other, or the passivation film also having the function of the light shielding film, and etching the amorphous silicon layer using the patterned passivation film and the drain electrode exposed outside the passivation film or the connection portion as the mask.

Other embodiments of the invention will be apparent to the skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is intended that the specification and examples be considered as exemplary only, with the true scope and spirit of the invention being indicated by the following claims.